VT6102

PCI FAST ETHERNET CONTROLLER WITH ACPI FUNCTION

DATA SHEET

(Preliminary)

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VIA TECHNOLOGIES, INC.

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1. Overview

1-1. VT6102 PCI FAST ETHERNET MAC CONTROLLER FEATURES

- **Single chip Fast Ethernet MAC controller for PCI bus interface**
  - -- Compliant to PCI 2.2 specification.
  - -- Provides a direct connection to PCI bus
  - -- Supports two network ports : 10/100MB MII interface

- **High performance PCI mastering structure**
  - -- VIA self-define 256 bytes memory I/O or register I/O based command and status register
  - -- Software oriented chain structure description to minimize hardware complexity
  - -- Include on chip bus master DMA with programmable burst length for high PCI bus utilization
  - -- Support Transmit data buffer byte-alignment for low CPU utilization
  - -- Dynamic transmit packet auto queuing for back to back transmissin
  - -- Programmable activity polling intervals for description DMA
  - -- Programmable DMA arbitration priority to minimize overflow under flow condition
  - -- Support early receive and early transmit interrupt for software parallel processing
  - -- Interrupt controllable by receive/transmit descriptor list for saving interrupt service time
  - -- PCI enhance command capable

- **Provides standard 100-M bits MII interface**
  - -- Support 100Base- T4 with CAT3, CAT4, CAT 5 UTP, STP
  - -- Support 100Base-TX with CAT5 UTP, STP and fiber cables
  - -- 10/100Mhz full duplex, half duplex operation

- **Separate 2K bytes FIFO for Receive and Transmit controllers**
  - -- both supports bursts of up to full Ethernet length
  - -- Programmable receive and transmit FIFO threshold control for optimize PCI throughput

- **Flexible dynamically load EEPROM algorithm.**
  - -- Load after power-up
  - -- Dynamic auto reload
  - -- Embedded programming for configure modification
  - -- Dynamic direct programming for manufacturing.

- **Support external Bootrom up to 64K bytes no external address latch**
  - -- Support Flash ROM read/write
  - -- Support EPROM Read.

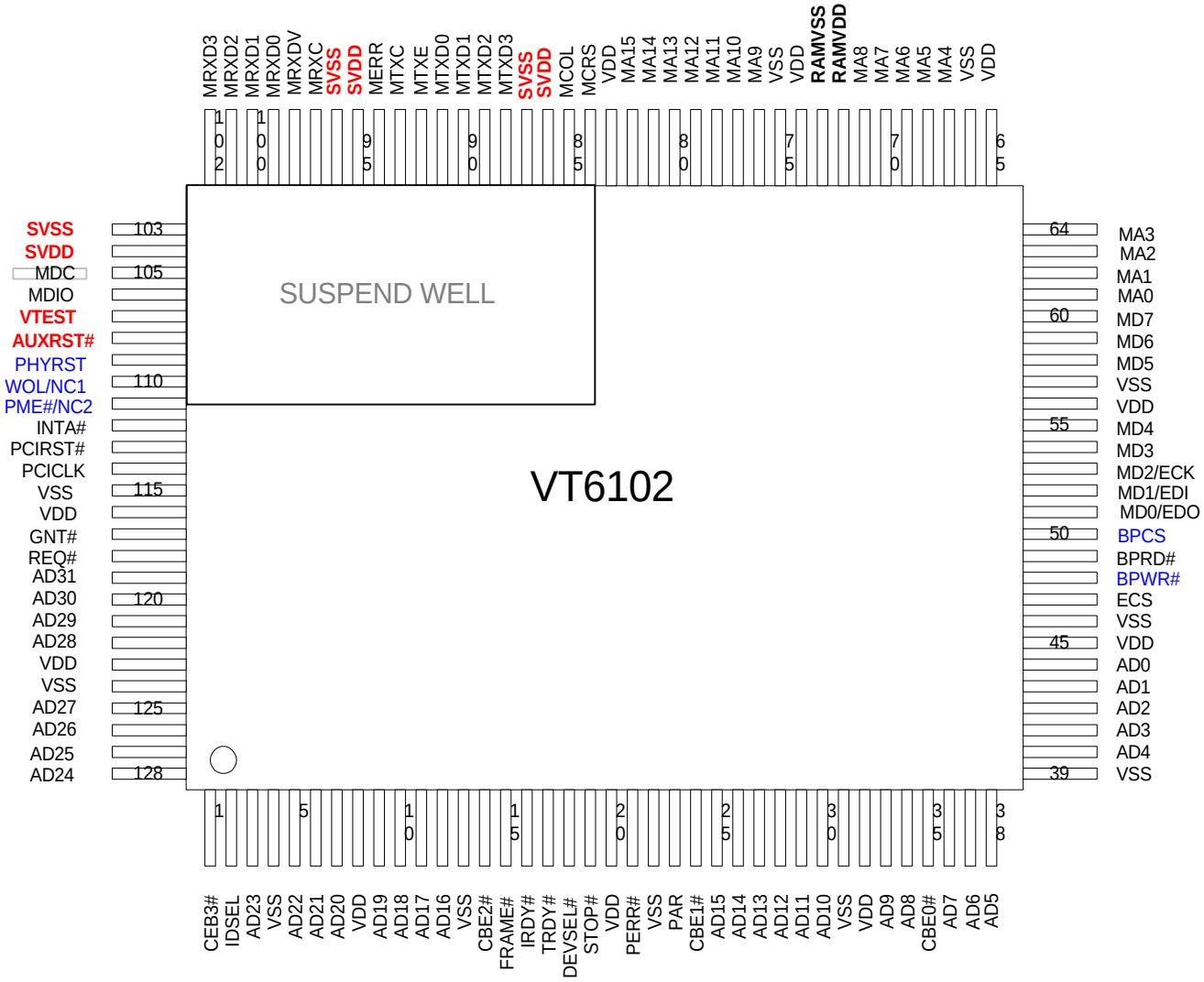
- **Support ACPI Functions**
  - -- Supports PC97, PC98, PC99 and Net PC requirements
  - -- Supports PCI Bus Power Management Interface Specification Version 1.0/1.1
  - -- Supports Advanced Configuration and Power Interface (ACPI) Specification 1.0
  - -- Supports Network Device Class Power Management Specification Version 1.0
  - -- Wake-up even support link change/magic packet/ unicast physical address/MS define pattern match

- **Support flow control functions**
  - -- Support IEEE802.3X for full duplex.
  - -- Support force Jam capable for half duplex.
  - -- multiple pause frame SON/SOFF.

- **Single 3.3V supply, 5.0V tolerant IO 0.35um triple metal CMOS technology**
- **128 pin PQFP package**

2. Pinouts

2-1. Pin Diagram



2-2. PIN LIST

Pin Name	Pin	Type	Pin Name	Pin	Type	Pin Name	Pin	Type
AD31	119	I/O	C/BE3#	1	I	MTXD3	88	O
AD30	120	I/O	C/BE2#	14	I	MTXD2	89	O
AD29	121	I/O	C/BE1#	24	I	MTXD1	90	O
AD28	122	I/O	C/BE0#	35	I	MTXD0	91	O
AD27	125	I/O	FRAME#	15	I/O	MTXE	92	O
AD26	126	I/O	IRDY#	16	I/O	MTXC	93	I
AD25	127	I/O	TRDY#	17	I/O	MERR	94	I
AD24	128	I/O	STOP#	19	I/O	MRXC	97	I
AD23	3	I/O	IDSEL	2	I	MRXDV	98	I
AD22	5	I/O	DEVSEL#	18	I/O	MRXD3	102	I
AD21	6	I/O	PAR	23	T/S	MRXD2	101	I
AD20	7	I/O	PCICLK	114	I	MRXD1	100	I
AD19	9	I/O	INTA#	112	OD	MRXD0	99	I
AD18	10	I/O	PCIRST#	113	I	MDC	105	O
AD17	11	I/O	GNT#	117	I	MDIO	106	IO
AD16	12	I/O	REQ#	118	O	VDD	8	VCC
AD15	25	I/O	PERR#	21	I/O	VDD	20	VCC
AD14	26	I/O	MA15	82	O	VDD	32	VCC
AD13	27	I/O	MA14	81	O	VDD	45	VCC
AD12	28	I/O	MA13	80	O	VDD	56	VCC
AD11	29	I/O	MA12	79	O	VDD	65	VCC
AD10	30	I/O	MA11	78	O	VDD	74	VCC
AD09	33	I/O	MA10	77	O	VDD	83	VCC
AD08	34	I/O	MA09	76	O	VDD	116	VCC
AD07	36	I/O	MA08	71	O	VDD	123	VCC
AD06	37	I/O	MA07	70	O	SVDD	86	VCC
AD05	38	I/O	MA06	69	O	SVDD	95	VCC
AD04	40	I/O	MA05	68	O	SVDD	104	VCC
AD03	41	I/O	MA04	67	O	VSS	124	GND
AD02	42	I/O	MA03	64	O	VSS	115	GND
AD01	43	I/O	MA02	63	O	VSS	75	GND
AD00	44	I/O	MA01	62	O	VSS	66	GND
VTEST	107	I	MA00	61	O	VSS	57	GND
PHYRST	109	O	MD7	60	I/O	VSS	46	GND
AUXRST#	108	I	MD6	59	I/O	VSS	39	GND
WOL/NC1	110	O	MD5	58	I/O	VSS	31	GND
PME#/NC2	111	O/D	MD4	55	I/O	VSS	22	GND
ECS	47	O	MD3	54	I/O	VSS	13	GND
BPCS#	50	O	MD2/ECK	53	I/O	VSS	4	GND
BPRD#	49	O	MD1/EDI	52	I/O	SVSS	103	GND
BPWR#	48	O	MD0/EDO	51	I/O	SVSS	96	GND
			MCRS	84	I	SVSS	87	GND
			MCOL	85	I	RAMVDD	72	VCC
						RAMVSS	73	GND

2-3. PIN DESCRIPTIONS

Signal Type Definition

Type	Name	Definition
I	Input	Input is a standard input-only signal.
O	Output	This is a standard active driver.
I/O	Input / Output	Thiis is an input/output signal
T/S	Tri-State	Tri-stae is a bi-directional, Tri-stae input/output pin
O/D	Open Drain	This allows multiple devices to share as a wire-OR

2-3-1. PCI Bus Interface

No.	Name	Type	Description
119-122, 125-128, 3,5,6,7,9, 10-12,25-30, 33,34,36-38 40-44	AD[31:0]	I/O	**Address and Data** are multiplexed on the same PCI pins. A bus transaction consists of an address phase followed by one or more data phases. The address phase is the clock cycle in which FRAME# is asserted. Write data is stable and valid when IRDY# is asserted and read data is stable and valid when TRDY# is asserted.
114	PCICLK	I	**PCI Clock** provides timing for all transactions on PCI and is an input pin to every PCI device.
112	INTA#	OD	**Interrupt** is an asynchronous signal which is used to request an interrupt
113	PCIRST#	I	**PCI Rest.** When PCIRST# is asserted low, the VT6102 chip performs an internal system hardware reset. PCIRST# may be asynchronous to CLK when asserted or deasserted. It is recommended that the deassertion be synchronous to guarantee clean and bounce free edge.
1 14 24 35	C/BE#[3:0]	I	**Bus Command/Byte Enables** are multiplexed on the same PCI pins. During the address phase of a transaction, CBE3-0B define the Bus Command. Burring the data phase, CBE3-0B are used as Byte Enables. The Byte Enables define which physical byte lanes carry meaningful data. CBE0B applies to byte 0 and CBE3B applies to byte 3.
2	IDSEL	I	**ID Select**.Used as a chip select during PCI configuration cycle.
15	FRAME#	I/O	**Frame**:.Cycle Frame is driven by the current master to indicate the beginning and duration of an access. FRAME# is asserted to indicate a bus transaction is beginning. While FRAME# is asserted, data transfers continue. When FRAME# is deasserted, the transaction is in the final data phase.
16	IRDY#	I/O	**Initiator Ready** indicates the initiating agent's ability to complete the current data phase of the transaction. IRDY# is used in conjunction with TRDY#. A data phase is completed on any clock when both IRDY# and TRDY# are asserted. During a write, IRDY# indicates that valid data is present on AD31-0. During a read, it indicates the master is prepared to accept data. Wait cycles are inserted until both IRDY# and TRDY# are asserted simultaneously.
17	TRDY#	I/O	**Target Ready** indicates the target's agent's ability to complete the current data phase of the transaction. TRDY# is used in conjunction with IRDY#. A data phase is completed on any clock when both IRDY# and TRDY# are asserted. During a read, TRDY# indicates that valid data is present on AD31-0. During a write, it indicates the target is prepared to accept data. Wait cycles are inserted until both IRDY# and TRDY# are asserted simultaneously.
18	DEVSEL#	I/O	**Device Select**, when actively driven, indicates the driving device has decoded its address as the target of the current access. As an input, DEVSEL# indicates whether any device on the bus has been selected.
19	STOP#	I/O	**Stop**: When VT6102 drives STOP# to disconnect further traction.
23	PAR	T/S	**Parity** is even parity across AD31-0 and CBE3-0B. PAR is stable and valid one clock after the address phase. For data phases PAR is stable and valid one clock after either IRDY# is asserted on a write transaction or TRDY# is asserted on a read transaction.
117	GNT#	I	**Bus grant** asserts to indicate to the VT6102 that access to the bus is granted.
118	REQ#	O	**Bus request** is asserted by the bus master indicate to the bus arbiter that it wants to use the bus.
21	PERR#	I/O	**Parity error** asserts when a data parity error is detected

2-3-2. Network Interface

No.	Name	Type	Description
85	MCOL	I	**Collision detect** when the external PHY device
84	MCRS	I	Carrier sense is asserted by the external PHY when the media is active
88-91	MTXD[3:0]	O	MII 4 parallel **transmit data lines**. This data be synchronized to assertion by the MTXC signal
92	MTXE	O	**Transmit enable** signals that the transmit is active in the MII port to an external PHY device
93	MTXC	I	**MII transmit clock** supports the 25mhz or 2.5mhz transmit clock supplied by the external PMD device. This clock should always be active.
94	MERR	I	**MII receive error** asserts when a data decoding error is detected by external PHY device.
97	MRXC	I	**MII receive clock** supports the 25mhz or 2.5mhz clock. This clock is recovered by the PHY.
98	MRXDV	I	MII data valid
99-102	MRXD[3:0]	I	Four parallel **receive data lines**. This data be driven from external PHY be synchronized with MRXC signal.
105	MDC	O	**MII management data clock** be soured by VT86C100A MDC bit (MIIR:0) to the external PHY devices as timing reference for the MDIO signal.
106	MDIO	I/O	**MII management data input/output,** read from MDI bit (MIIR:1) or written from MDO bit (MIIR:2)

2-3-3. EEPROM Interface

No.	Name	Type	Description
47	ECS	O	**EEPROM Chip Select**: Chip select signal for the external EEPROM when a EEPROM is used to provide the configuration data and Ethernet Address. A 100K pull-up resistor is connected.
48	BPWR#	O	**Boot ROM Write enable,** it's provides the active low output control to the flash
49	BPRD#	O	**Boot ROM Read**: Read the Boot ROM on the memory support data bus.
50	BPCS#	O	**Boot ROM chip select** on local memory data bus.
51	MD0/ EDO	I/O I	**Bootrom data** bus 0 Serial ROM Data output
52	MD1/ EDI	I/O O	**Bootrom data** bus 1 Serial ROM Data input
53	MD2/ ECK	I/O O	**Bootrom data** bus 2 Serial ROM Clock signal
54 55 58 59 60	MD3 MD4 MD5 MD6 MD7	I/O	**Bootrom data** bus [3-7]
82-61	MA[15:0]	O	**Bootrom address** line [15-0]

2-3-4. Power Management interface

No.	Name	Type	Description
110	WOL	O	**Wake on Lan Event,**,programmable pulse or button WOL event, active high.
111	PME#	O/D	**Power management event**.interrupt outpur
108	AUXRST#	I	**PHY reset aux input.** This pins might connect to PCI reset for non-wake on LAN design. This pins is normally no connect or pull up with 22 ohm resistor.
109	PHYRST	O	**PHY RESET Pin,** PHY reset output to external PHY device. This output polarity control by VTEST, When VTEST=0,PHY reset high active, When VTEST=1,PHY reset low active.
107	VTEST	I	**Test control Pin,**it can control PHY reset output polarity

2-3-5. Power and Ground

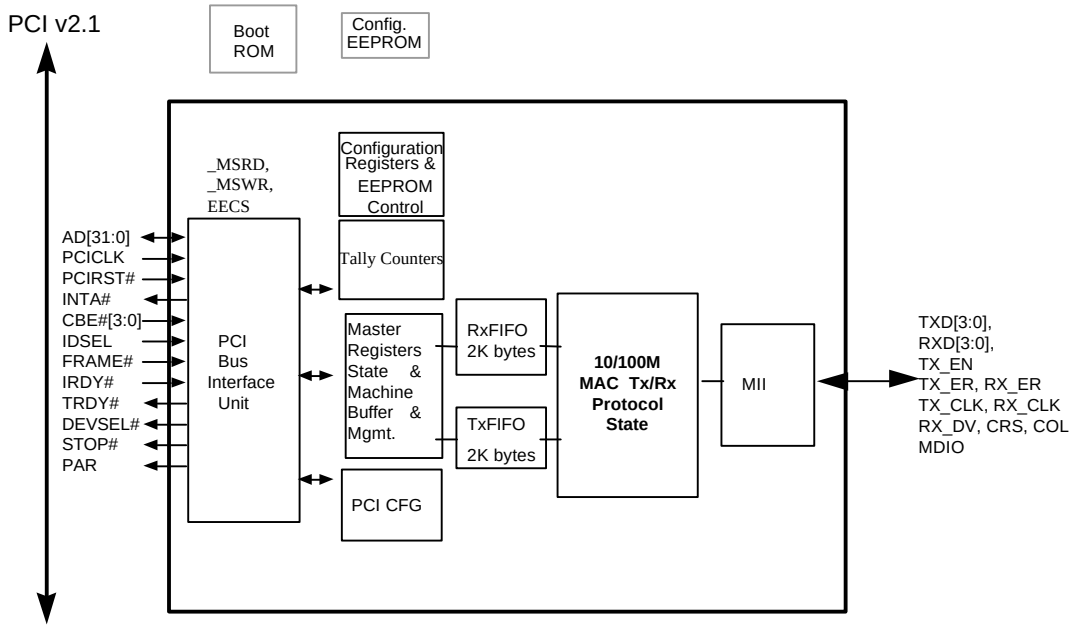
No.	Name	Type	Description
8,20,32, 45,56,65, 74,83,1 16,123	VDD	P	VCC Power: +3.3V
86,95,104	SVDD	P	Standby VCC Power: +3.3V
4,13,22, 31,39,46, 57,66,7 5,115, 124	VSS	G	Ground: 0V
87,96,103	SVSS	G	Ground: 0V
72	RAMVDD	P	Memory Interface Power
73	RAMVSS	G	Memory Interface Ground

3. FUNCTION DESCRIPTION

3-1. GENNRAL DESCRIPTION

The VT6102 ACPI **PCI bus master** 100 M FAST Ethernet controller is CMOS VLSI designed for easy implementation of CSMA/CD IEEE 802.3u 100M local area networks. Significant features include: twisted-pair interface, PCI Plug&Play compatibility, 32 bit bus mastering, powerful buffer management and Early Interrupt Receive/Transmit.

The VT6102 integrates the entire bus interface of PCI systems. Setting hardware jumpers or software configures the VT6102 bus interface. The VT6102 also complies with PCI Specification v2.1. The VT6102 supports the Media Independent Interface (MII) network interface.



3-1-1. FIFO and control logic

The VT6102 incorporates two independent 2K bytes deeper FIFO for transmit or received data from system interface or to the network interface, providing temporary storage of data, free host system from the real-time demands on network. The VT6102 enhanced the FIFO management logic to handle received data packets up to four packets before transfer to system data buffer. This ability reduce the packets losing due to PCI bus mastering abrition latency.

3-1-2. Network interface

The VT6102 ACPI support one MII interface

3-2. MII INTERFACE

The MII interface is an IEEE 802.3 compliant interface that provides a simple and easy interconnection between the MAC layer and PHY device. This interface has support the following characteristics:

- Support both 10M and 100M data rate.
- Contains data and synchronous clock
- 4-bit independent receive and transmit data.
- Uses TTL signal levels and compatibles with common CMOS processes.

3-3. EEPROM INTERFACE

ETHER_ID1	ETHER_ID0	00H
ETHER_ID3	ETHER_ID2	01H
ETHER_ID5	ETHER_ID4	02H
Reserved	MII_ PHY AD	03H
SUB_SID1	SUB_SID0	04H
SUB_VID1	SUB_VID0	05H
Reserved	Reserved	06H
Reserved	Reserved	07H
Data_SEL	PMCC	08H
Reserved	PMU_DATA_REG	09H
Reserved	Reserved	0AH
Max_LAT	Min_GNT	0BH
BCR1	BCR0	0CH
CFG_B	CFG_A	0DH
CFG_D	CFG_C	0EH
CHKSUM	73H	0FH

3-3-1. Direct Programming of EEPROM

The VT6102 features a easy way to program external EEPROM in-situ. When the RESET is active and if the upper byte of 0FH on EEPROM is not 73H, the EEPR bit will not be set to indicate that the current EEPROM has not been programmed yet. This will allow the VT6102 to enter Direct Programming mode if EELOAD is also set. In this mode the user can directly control the EEPROM interface signals by writing to the ECSR Port and the value on the EECS, ESK and EDI bits will be driven onto the EECS, SK(MD2), and DI(MD1) outputs respectively. These outputs will be latched so the user can generate a clock on SK by repetitively writing 1 then 0 to the appropriate bit. This can be used to generate the EEPROM signals as per the 93C46 data sheet.

To read the EEPROM data, users have to generate EEPROM interface signals into EECS, DI and SK as described above and in the mean time read the data from DO(MD0) input via pin SD0. Reading Data Transfer Port during programming will not affect the latched data on EECS, SK, and DI outputs. When the EEPROM has been programmed and verified (remember to program the upper byte of 0EH & 0FH with 73H), the user must give VT6102 a power-on reset to return to normal operation and to read in the new data.
The Direct Programming mode is mainly used for production to program every bit of the EEPROM. Once the upper byte of 0EH has been programmed with 073H and a power-on reset has been performed, there is no way to change the contents of EEPROM except Configuration Registers A, B, and C, which will be discussed in the following paragraph. For more information, refer to EECSR.

3-3-2. EMBEDDED PROGRAMMING OF EEPROM

If the upper byte of 0FH of EEPROM has been programmed to 073H when VT86C100A is loading the EEPROM data during power-on reset, the EEPR bit of Signature Register will be set to prohibit the Direct Programming mode. However, the user can still program the configuration registers A, B, and C using the Embedded Programming mode by following the routine specified in the pseudo code below. This operation will work regardless of the value of EECONFIG. The setting of the EELOAD bit of Configuration Register B starts the EEPROM write process. Care should be taken not to accidentally modify the POL and GDLNK bits because these two bits return the value indifferent from the setting. This programming process is ended when the EELOAD bit goes to zero.

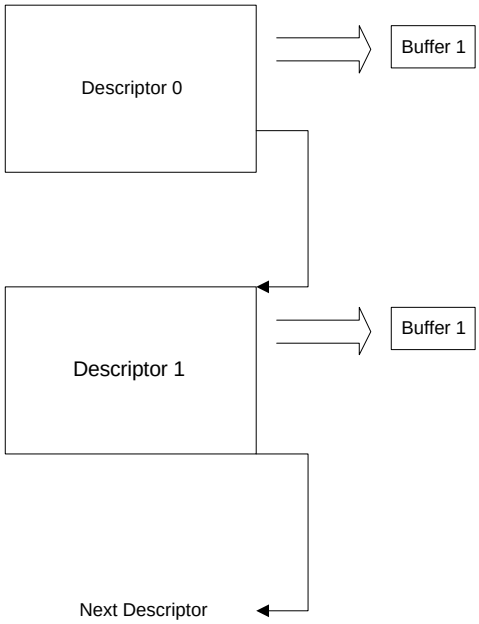
```
EEPROM_EMB_PROG ( )
{       //      defined constant: CONFIG_B,    EELOAD
        //      declared register: value, config_for_A, config_for_B, config_for_C
        //      declared function: DISABLE_INTERRUPTS, ENABLE_INTERRUPTS, READ, WRITE, WAIT
        DISABLE_INTERRUPTS ( );
        value = READ (CONFIG_B);
        value = value | EELOAD;
        WRITE (CONFIG_B, value);
        READ (CONFIG_B);
        WRITE (CONFIG_B, config_for_A);
        WRITE (CONFIG_B, config_for_B);
        WRITE (CONFIG_B, config_for_C);
        while (value || EELOAD)
        {
                value = READ (CONFIG_B);
                WAIT ( );
        }
        ENABLE_INTERRUPTS ( );
}
```

3-4. BUFFER MANAGEMENT & HOST COMMUNICATION

The VT6102 provides an simply and effective buffer management and host communication method through the PCI Bus master: There are two descriptor lists, one for receive and one for transmit. The base of these two list are pointed into the CRDA (18h) and CTDA (1ch) registers.

The descriptor list reside in the host physical memory address space with **double word boundary**. And each descriptor lists just point to one single buffer, but a data buffer consists of either an entire frame or part of a frame. Data chain can be enabled or disabled by DES1 C bit. Data buffer also reside in host physical memory double word boundary space.

The device driver can make the last descriptors next link be point to first descriptor address, become a ring buffer structure.

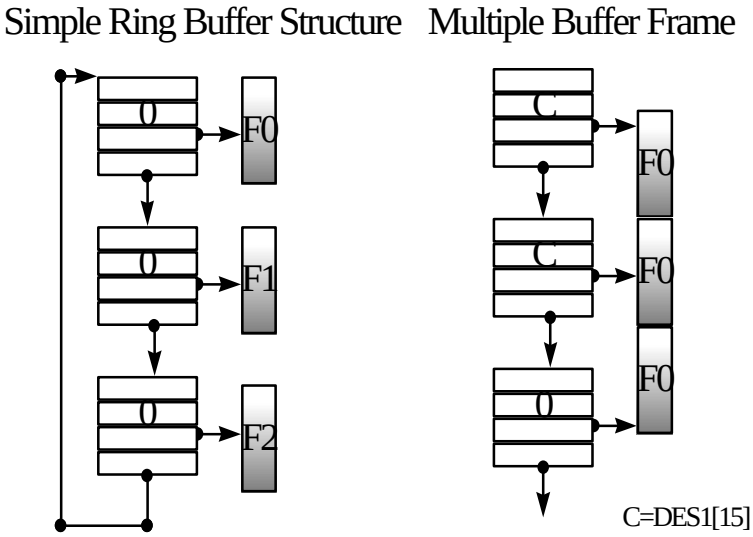


3.5 BUFFER STRUCTURE AND INTERRUPT CONTROL

A data consists of an entire frame or part of a frame, but it cannot exceed a single Ethernet frame size. Buffers contain only data; All buffer status is maintained in the descriptor . Data chaining can be enable or disable by Chain bit in DES1[15]. The interrupt control also can be enable or disable by DES1[23]

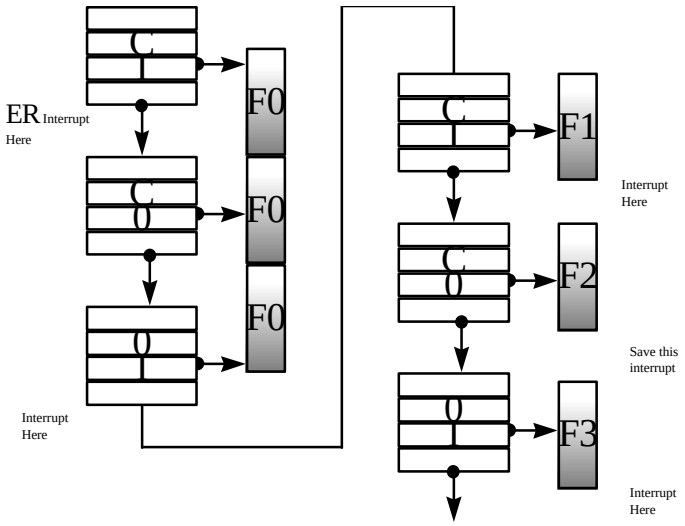
3-5-1 Multiple Chained buffer structure

The VT6102 can support multiple chain buffer for direct map to OS`s data buffer. The VT6102 bus mastering module will direct move the data from network to the OS`s data buffer or direct transmit the data in OS`s buffer onto network not necessary move to a temperate data buffer. But the data buffer must be double word aligned. In this multiple chained buffer structure, the first data buffer' s descriptor Chain



3-5-2 Interrupt Control

The VT6102 can controllable the receive descriptors and transmit descriptor for what the interrupt occurred.
The IC bit (DES1[23]) be set 1, the receive or transmit interrupt will be generate the interrupt no matter the frame been complete received or transmitted. This feature will enable the OS pre-fetch the frame header or saving the interrupt service overload.



3-5. FLOW CONTROL

The VT6102 support flow control in both half duplex and full duplex. In half duplex mode, VT6102 support jam based flow control, when traffic busy, MAC will send jam pattern. In full duplex mode, the pause frame detection logic operate base on the flow control register 0x80, if this flow control bit is set to enable, The Vt6102 will detect PAUSE frame.

3-6. POWER MANAGEMENT

The VT6102 support ACPI Specification V1.0 and Network device class power management, and PC97/PC98/PC99 and net PC requirements, four wake-up evens are Support in VT6102 and can wake up the system when it received a frame that qualifies as a wake-up packet.

3-6-1. Wake up events

- Link status change
  - If this link state have change connect or disconnect and *PMEOVR* bit (0x83/bit 7) enable, PME# will be generated when link state change.

- Magic packet
  - When VT6102 is set to magic packet mode, it require that a received packet qualify as a Magic Packet The Magic packet pattern 6 FFh byte + SA duplication 16 times destination address of received magic packet matches, meanwhile Magic register (0xA0/bit 5) set enable, VT6102 will received this packed.

- Unicast phisical address match
  - When VT6102 is set to unicast mode, it require that a received packet qualify as a unique individual address and unicast register bit (0xA0/bit 5) set enable, VT6102 will received this packed.

- MS defined pattern match
  - IP (ARP)
  - Name Query
  - NET BIOS
  - VIA defined

3-6-2. Power states

VT6102 Device state	Condition	I_PCI mA	I_AUX mA	Action From Function
D0	PCI=33, MAC=25M Tx,Rx Active	28	11	Any PCI transaction or interrup
D1,D2	PCI=33M, MAC=25M PCI bus transaction IDLE	18	9	Wake up event
D3 hot	PCICLK IDLE, MAC=25M TX off, RX on	9	8	Wake up event
D3 cold	PCI power off,MAC=25M Tx off, RX on	9	8	Wake up event

4. REGISTERS

4-1. PCI CONFIGURATION REGISTER

31 16 15 0

Device ID **(3065)**		Vendor ID **(1106)**		00H
Status		Command		04H
Class Code			Revision ID	08H
BIST	Header Type	Latency Timer	Cache Size	0CH
Base Address Registers				10H
				14H
				18H
				1CH
				20H
				24H
Card Bus CIS Pointer(00)				28H
SUB-System ID		SUB-Vendor ID		2CH
Expansion ROM Base Address				30H
Reserved			Cap_Ptr	34H
Reserved				38H
Max_Lat	Min_Gnt	Interrupt Pin	Interrupt Line	3CH
Power Management Capabilities (PMC)		Next Item Ptr	Capability ID	40H
Data	PMCSR_BSE Bridge support Extensions	Power Management Control/Status Register (PMCSR)		44H
Reserved	Rserved	Reserved	Rserved	50H
Reserved	Rserved	Reserved		50H

4-1-1. PCI Configuration description (00-05H)

OFFSET	Bit	Symbol	Description	Default	ACC
00-01H	0-15	Vendor ID	This field identifies the manufacturer of device.	1106	RO
02-03H	16-31	Device ID	This field identifies the particular of device.	3043	RO
04-05H	0	Command	IO space enable	0	RW
04-05H	1	Command	Memory space enable	0	RW
04-05H	2	Command	BUS master enable	0	RW
04-05H	3	Command	Special cycles enable	0	RW
04-05H	4	Command	Memory write and invalidate enable	0	RW
04-05H	5	Command	VGA palette snoop	0	RW
04-05H	6	Command	Parity error response	0	RW
04-05H	7	Command	Wait cycle control	0	RW
04-05H	8	Command	SERR# enable	0	RW
04-05H	9	Command	Fast back to back enable	0	RW
04-05H	10-15	Command	Reserved.	0	RW

4-1-2.PCI Configuration description (06-4FH)

OFFSET	Bit	Symbol	Description	Default	ACC
06-07H	0-3	Status	Reserved	0	RO
06-07H	4	Status	Capabilities, such as PCI power management.	1	RO
06-07H	5	Status	66 MHz Capable	0	RO
06-07H	6	Status	UDF supported	0	RO
06-07H	7	Status	Fast back-to-back capable	1	RO
06-07H	8	Status	Data parity error detected	0	RO
06-07H	9-10	Status	DEVSEL timing ,00-fast,01-medium,10-slow	10b	RO
06-07H	11	Status	Signaled target abort	0	RO
06-07H	12	Status	Received target abort	0	RO
06-07H	13	Status	Received master abort	0	RO
06-07H	14	Status	Signaled system error	0	RO
06-07H	15	Status	Detected parity error	0	RO
08H	0-7	Revision ID	This register a device specific revision identifier	40h	RO
09-0BH	8-31	Class code	The register is used to identify the generic function of the device and specific register-level programming interface.		RO
0CH	0-7	CacheLine Size	This register must be implement by master devices that can generate the memory write and invalidate command.		RW
0DH	8-15	Latency Timer	This register must be implemented as writable by any master that can burst more than two data phase.		RW
0EH	16-23	Header Type	Refer to PCI 2.1 SPEC		RO
0FH	24-31	BIST	Built in self test		RO
34H	0-7	The Cap_Ptr	The register provides an offset into the function's PCI configuration space for the location of the first item in the Capabilities linked list		RO
40H	0-7	Cap ID	When set 01 identifies the linked list item as being the PCI power Management registers.	01	RO
41H	0-7	Netx item pointer	This field provide an offset into the function's PCI configuration space pointing to the location of next item in the function's capability list	0	RO
42-43H	0-2	Version	A value of 010b indicates that this function complies with revision 1.1 of the power management interface specification.	010b	RO
42-43H	3	PME CLK	PMECLK=1, relies to PCI clock for PME# operation PMECLK=0, no PCI clock is require for the function to generate PME#.	0b	RO
42-43H	4	Reserved			
42-43H	5	DSI	The device specific initialization bit		RO
42-43H	6-8	AUX_Curr	This 3 bit field reports the 3.3Vaux auxiliary current requirement for the PCI function..refer to PM11 Spec		RO
42-43H	9	D1 Support	If this bit a 1,this function support D1 PM state		RO
42-43H	10	D2 Support	If this bit a 1,this function support D2 PM state		RO
42-43H	11-15	PME_Supp	This 5 bit field indicates the power state in which the function may assert PME#. Bit11 XXXX1b – PME# can be asserted from D0 Bit12 XXX1Xb – PME# can be asserted from D1 Bit13 XX1XXb – PME# can be asserted from D2 Bit14 X1XXXb – PME# can be asserted from D3h Bit15 1XXXXb – PME# can be asserted from D3c		RO
44-4F	0-31	PMCSR	Refer to Power Management spec 1.0		RWC

4-2. VT6102 INTERNAL REGISTER MAP

PAR3	PAR2	PAR1	PAR0	00H
TCR	RCR	PAR5	PAR4	04H
Reserved	Reserved	CR1	CR0	08H
IMR1	IMR0	ISR1	ISR0	0CH
MAR3	MAR2	MAR1	MAR0	10H
MAR7	MAR6	MAR5	MAR4	14H
CURR_RX_DESC_ADDR				18H
CURR_TX_DESC_ADDR				1CH
GFSTATUS	TFTCMD	RFTCMD	GFTEST	54H
CURR [8:0]		BNRY [8:0]		58H
FIFIO DATA PORT				5CH
Tally counter test port				68H
BCR1	BCR0	MIISR	PHY_ADR	6CH
MII DATA REG		MIIADR	MIICR	70H
DEBUG1	DEBUG0	TRST	EECSR	74H
CFGD	CFGC	CFGB	CFGA	78H
Tally Counter_CRC		Tally counter_MPA		7CH
STICKHW	PMCPORT	MISC.CR		80H
Reserved	MIMR	Reserved	MISR	84H
Reserved				88H
BPMD	0	BPMA [15:0]		8CH
EE_CHKSUM	0	BPIN_DATA	BPCMD	90H
0	SU_PHYID	SUSPEND MII_AD		94H
0000_00_0_pauseSR		PAUSE TIMER		98H
SOFT_TIMER_1		SOFT_TIMER_0		9CH
WOLCG.SET	TESTREG	PWCFG.SET	WOLCR.SET	A0H
WOLCG.CLR	TESTREG	PWCFG.CLR	WOLCR.CLR	A4H
Reserved			PWRCSR.SET	A8H
Reserved			PWRCSR.CLR	ACH
PATTERN_CRC0 [31:0]				B0H
PATTERN_CRC1 [31:0]				B4H
PATTERN_CRC2 [31:0]				B8H
PATTERN_CRC3 [31:0]				BCH
BYTEMSK0 [31:0]				C0H
BYTEMSK0 [63:32]				C4H
BYTEMSK0 [95:64]				C8H
BYTEMSK0 [127:96]				CCH
BYTEMSK1 [31:0]				D0H
BYTEMSK1 [63:32]				D4H
BYTEMSK1 [95:64]				D8H
BYTEMSK1 [127:96]				DCH
BYTEMSK2 [31:0]				E0H
BYTEMSK2 [63:32]				E4H
BYTEMSK2 [95:64]				E8H
BYTEMSK2 [127:96]				ECH
BYTEMSK3 [31:0]				F0H
BYTEMSK3 [63:32]				F4H
BYTEMSK3 [95:64]				F8H
BYTEMSK3 [127:96]				FCH

4-2-1. VT6102 internal register description (00-07H)

OFFSET	Bit	Symbol	Description	Default	ACC
0-5H	0-63	PAR0-5	**Ethernet address**		RW
			RCR		
06H	0	SEP	**Error Packets Accepted** If SEP=0, packet with receive errors are rejected. If SEP=1, packet with receive errors are accepted.	0	RW
06H	1	AR	**Small packets Accepted** If AR=0,packet smaller than 64 byte are rejected. If AR=1,packet smaller than 64 byte are accepted.	0	RW
06H	2	AM	**Multicast packets accepted** If AM=0, packet with multicast are rejected. If AM=1, packet with multicast are accepted	0	RW
06H	3	AB	**Broadcast Packets Accepted** If AB=1,packet with broadcast are accepted. If AB=0,packet with broadcast are rejected.	0	RW
06H	4	PROM	**Physical address packets accepted** If PROM=0,physical address must match node address in PAR0-5. If PROM=1,all packet with physical destination address are accepted.	0	RW
06H	5	RRFT0	**Receive FIFO Threshold** 000----------64 byte 001----------32 byte 010----------128 byte 011----------256 byte 100----------512 byte 101----------768 byte 110----------1024 byte 111----------store & forward	000	RW
06H	6	RRFT1			
06H	7	RRFT2			
			TCR		
07H	0	RESV	**Reserved**	0	RW
07H	1	LB0	**Transmit Loopback mode** 00----------Normal 01----------Internal loopback (MAC only) 10----------MII loopback(MAC-PHY) 11----------223 or other loopback	00b	RW
07H	2	LB1			
07H	3	OFSET	Back-off priority selection If OFSET =0,VIA back off algorithm If OFSET =1,National specification compatible backoff algorithm	1	RW
07H	4	RESV	**Reserved**	0	RW
07H	5	RTSF0	**Transmit FIFO Threshold (Mode10T)** 000----------128 byte----------64byte 001----------256 byte----------128 byte 010----------512 byte----------256 byte 011----------1024byte----------512 byte 1xx----------store & forward	000	RW
07H	6	RTSF1			
07H	7	RTSF2			

4-2-2.VT6102 internal register description (08-09H)

OFFSET	Bit	Symbol	Description	Default	ACC
CR0					
08H	0	INIT	**INIT** process begin	0	RW
08H	1	STRT	**Start NIC** If Start=0,no command entered. If Start=1,start processing a command.	0	RW
08H	2	STOP	**Stop NIC** If Stop=0,command processing is in process If Stop=1,no command processing is in process	0	RW
08H	3	RXON	**Receive process** If RXON=0,no in receive state If RXON=1,turn on the receive DMA state	0	RW
08H	4	TXON	**Transmit process** If TXON=0,no in transmit state If TXON=1, turn on the transmit DMA state	0	RW
08H	5	TDMD	**Transmit poll demand** If TDMD=1,set 1 to poll the TD once, it will be cleared by itself after polling complete.	0	RW
08H	6	RDMD	**Receive poll demand** If TDMD=1,set 1 to poll the RD once, it will be cleared by itself after polling complete.	0	RW
08H	7	RESV	**Reserved**		
CR1					
09H	0	EREN	**Early receive enable** If EREN=0, disable early receive mode If EREN=1, enable early receive mode.	0	RW
09H	1	RESV	**Reserved**	0	RW
09H	2	FDX	Full duplex If FDX=0,set MAC to half duplex mode If FDX=1, set MAC to full duplex mode	0	RW
09H	3	DPOLL	**Disable TD/RD auto polling** If Dpoll=0,set TX/RX auto polling enable. If Dpoll=1,set TX/RX auto polling disable.	0	RW
09H	4	RESV	**Reserved**	0	RW
09H	5	TDMD1	**Transmit poll demand 1** If TDMD=1,set 1 to poll the TD once, it will be cleared by itself after polling complete.	0	RW
09H	6	RDMD1	**Receive poll demand 1** If TDMD=1,set 1 to poll the RD once, it will be cleared by itself after polling complete.	0	RW
09H	7	SFRST	**Software reset** If SFRST=0,normal condition If SFRST=1,software reset. It will be cleared after software rest complete.	0	RW

4-2-3. VT6102 internal register description (0C-1FH)

OFFSET	Bit	Symbol	Description	Default	ACC
ISR0					
0CH	0	PRX	Received a packet successfully	0	RW
0CH	1	PTX	Transmitted a packet successfully	0	RW
0CH	2	RXE	**Receive error** When this bit is set, MAC received with the following errors 1.CRC error 2.Frame alignment error 3.fifo overflow 4.RD linking error.	0	RW
0CH	3	TXE	**Transmit error** When this bit is set, packet transmitted is abort due to 1.excessive collision. 2.Txmit underflow 3.TD linking error	0	RW
0CH	4	TU	Transmit buffer underflow	0	RW
0CH	5	RU	Receive buffer link error	0	RW
0CH	6	BE	PCI Bus error	0	RW
0CH	7	CNT	CRC or miss packet tally counter overflow.	0	RW
ISR1					
0DH	0	ERI	Early receive interrupt	0	RW
0DH	1	UDFI	TX FIFO underflow event	0	RW
0DH	2	OVFI	Receive FIFO overflow	0	RW
0DH	3	PKT Race	FIFO overflow condition, it's mean next packet race with current packet	0	RW
0DH	4	NORBF	No more receive buffer to be used	0	RW
0DH	5	ABTI	Transmit abort interrupt because of excessive collision	0	RW
0DH	6	SRCI	Port state change	0	RW
0DH	7	GENI	General purpose Interrupt	0	RW
0EH	0-7	IMR0	Interrupt mask register 0, all bit correspond to the bits in the ISR0 register.	0	RW
0FH	0-7	IMR1	Interrupt mask register 1, all bit correspond to the bits in the ISR1 register.	0	RW
10-17H	0-63	MAR0-7	Multicast address	0	RW
18-1BH	0-31		Curr_RX_DESC_Address	0	RW
1C-1FH	0-31		Curr_TX_DESC_Address	0	RW

4-2-4. VT6102 internal register description (20-2FH)

O	0	0	0	0	Length [10:0]					RSR1				RSR0		RDSE0
Reserved								Reserved		**C**	0	0	0	0	RX_Buffer_Size [10:0]	RDSE1
RX DATA BUFFER START ADDRESS																RDSE2
RD BRANCH ADDRESS																RDSE3

OFFSET	Bit	Symbol	Description	Default	ACC
RDSE0-RSR0					
20H	0	RERR	Receiver error		RO
20H	1	CRC	CRC error		RO
20H	2	FAE	Frame alignment error		RO
20H	3	FOV	FIFO overflow		RO
20H	4	LONG	A Long packet		RO
20H	5	RUNT	A run packet		RO
20H	6	SERR	System error		RO
20H	7	BUFF	Buffer underflow error		RO
RDSE0-RSR1					
21H	8	EDP	End of packed buffer		RO
	9	STP	**Packet start** STP EDP 1 1-------- Single buffer descriptor 1 0-------- The start descriptor of chain buffer 0 1-------- The end descriptor of chain buffer 0 0-------- The start middle descriptor of chain buffer		RO
	10	CHN	Chain buffer	1	RO
	11	PHY	NIC accept Physical address packet		RO
	12	BAR	NIC accept broadcast packet		RO
	13	MAR	NIC accept multicast packet		RO
	14	RESV	Reserved		RO
	15	RXOK	Received packed successfully		RO
22-23H	16-26	Length	Received packet length		RO
23H	27-30	0000	Extend byte count for abnormal size Ethernet frame.		RO
23H	31	O	**Owner bit,** set by driver at initialization. If OWN=0, descriptor is owed by host. If OWN=1,descriptor is owned by NIC		RW
RDSE1					
24-25H	0-10	RBS	**RX_ Buffer Size** Receive buffer size for this descriptor, the total byte count of the whole frame will be store in the last descriptor.		RO
	11-14	0000	Must be zero		
	15	C	Chain buffer		
26-27H	16-31	RESV	Reserved		
RDSE2					
28-2BH	0-31	RDSE2	RX DATA BUFFER START ADDRESS		RO
RDSE3					
2C-2FH	0-31	EDSE3	RD BRANCH ADDRESS		RO

4-2-5. VT6102 internal register description (40-4FH)

O	Reserved									TSR1					TSR0		TDSE0
Reserved							TCR	**C**	0	0	0	0	TX_Buffer_Size [10:0]				TDSE1
TX DATA BUFFER START ADDRESS																	TDSE2
TD BRANCH ADDRESS																TDCTL [3:0]	TDSE3

OFFSET	Bit	Symbol	Description	Default	ACC
TDSE0-TSR0					
40H	0-3	NCR0-3	Collision retry count		RO
	4	COLS	Experience collision in this transmit event.		RO
	5	RESV	Reserved		RO
	6	RESV	Reserved		RO
	7	CDH	CD hearbeat, this bit only effective in 10base-T mode, when Set this bit indicates a hearbeat collision check failure.		RO
TDSE0-TSR1					
41H	8	ABT	Transmit abort after excessive collision		RO
	9	OWC	Out of window collision seen		RO
	10	CRS	Carrier sense lost when transmitting		RO
	11	UDF	TX FIFO underflow even.		RO
	12	TBUFF	Invalid TD format or structure or TD underflow		RO
	13	SERR	System error		RO
	14	RESV	Reserved		RO
	15	TERR	**Transmit error** If TERR=0,transmit successful If TERR=1,excessive collision (COL16TM)		RO
42-43H	16-30	RESV	Reserved		RO
	31	O	**Owner bit,** set by driver at initialization. If OWN=0, descriptor owned by host. If OWN=1,descriptor owned by NIC		RW
TDSE1					
44-45H	0-10	TBS	**TX_ Buffer Size** Transmit packet buffer size for this descriptor, the total byte count of the whole frame will be store in the last descriptor.		RO
44-45H	11-14	0000	Extend fragment of frame length, must be zero.		RO
44-45H	15	C	Chain buffer		RO
TDSE1-TCR					
46-47H	16	CRC	Disable CRC generation		RO
	17-20	RESV	Reserved		RO
	21	STP	Start of transmit packet		RO
	22	EDP	End of transmit packet		RO
	23	IC	Assert interrupt immediately while the descriptor has been Send complete.		RO
	24-31	RESV	Reserved		RO
TDSE2					
48-4BH	0-31	TDSE2	TX DATA BUFFER START ADDRESS		RO
TDSE3					
4CH	0	TDCTL	If this bit set to 0, issue interrupt for this packet If this bit set to 1, no interrupt generated		RO
4CH	1-3	TDCTL	Received		RO
4C-4FH	4-31	TDSE3	TD BRANCH ADDRESS		RO

4-2-6. VT6102 internal register description (6C-6FH)

OFFSET	Bit	Symbol	Description	Default	ACC
PHY_ADR					
6CH	0-4	PHYAD	**Extend PHY device address** These register bytes store from EEPROM loading when power up or EEPROM auto-reloading , it's can be programmed by software.	00001b	RW
6CH	5	MFDC	**Accelerate MDC speed** If MFDC=0,MDC=normal If MFDC=1,MDC=4X accelerating	0	RW
6CH	6	MPO0	**MII management polling timer interval**	00	RW
6CH	7	MPO1	00----------1024 MDC clock cycles 01----------512 MDC clock cycles 10----------128 MDC clock cycles 11----------64 MDC clock cycles		
MIISR					
6DH	0	SPD10	**PHY Speed** If SPD10=0, speed at 100MB If SPD10=1, speed at 10 MB	1	RW
6DH	1	LNKFL	**Link Fail** If LNKFL=0, link success. If LNKFL=1, link fail that no cable is connect.	1	RW
6DH	2	RESV	Reserved	0	RW
6DH	3	MIIERR	PHY device received error.	0	RW
6DH	4	PHYOPT	PHY option If PHYOPT=0, PHY address will be update by EEPROM If PHYOPT=1, use default PHY address as 0001b.	1	RW
6DH	5	RESV	Reserved	0	RW
6DH	6	RESV	Reserved	0	RW
6DH	7	PHYRST	PHY reset, by software driven.	0	RW
BCR0					
6EH	0	DMA0	**DMA Length**	0	RW
6EH	1	DMA1	000----------32 byte----------8 DW		
6EH	2	DMA2	001----------64 byte----------16 DW 010----------128 byte----------32 DW 011----------256 byte----------64 DW 100----------512 byte----------128 DW 101----------1024 byte----------256 DW 110----------store & forward 111----------store & forward		
6EH	3	CRFT0	If CRFT2,CRFT1,CRFT0=0,0,0 then RXFIFO threshold control is determined by RCR, else it is determined by BCR0	0	RW
6EH	4	CRFT1			
6EH	5	CRFT2			
6EH	6	EXTLED	Extra LED support control	0	RW
6EH	7	MED2	Medium select control	0	RW
BCR1					
6FH	0	POT0	Polling timer interval.	0	RW
6FH	1	POT1			
6FH	2	POT2			
6FH	3	CTFT0	If CTFT2,CTFT1,CTFT0=0,0,0 then TXFIFO threshold control is determined by TCR, else it is determined by BCR1	0	RW
6FH	4	CTFT1			
6FH	5	CTFT2			

4-2-7. VT6102 internal register description (70-77H)

OFFSET	Bit	Symbol	Description	Default	ACC
MIICR					
70H	0	MDC	Direct programming status as management port clock		RW
70H	1	MDI	Direct programming input while read PHY status		RW
70H	2	MDO	Direct programming status as management port data out		RW
70H	3	MOUT	MDIO out put enable indicator.		RW
70H	4	MDPM	**Direct PHY programming mode enable** If MDPM=1,WCMD & RCMD have no effect		RW
70H	5	WCMD	Write enable to write PHY, reset while write complete		RW
70H	6	RCMD	Read enable to read PHY, reset while read complete and PHY Status is store in 0x72H		RW
70H	7	MAUTO	**MII management port auto polling enable.** MIICR has no effect while MAUTO=1		RW
MIIADR					
71H	0	MAD0	MII management port address bit [4:0]	0001b	RW
71H	1	MAD1			
71H	2	MAD2			
71H	3	MAD3			
71H	4	MAD4			
71H	5	MDONE	A pause status/control bit, when MDIO auto polling data is ready, It's mean MII state of SM is at the end of a auto polling cycle.		RW
71H	6	MSRCEN	If MSRCEN=1, close the pause function of MDONE		RW
71H	7	MIDLE	If MIDLE=1, has not at MII auto polling cycle.		RO
EECSR					
74H	0	EDO	Direct program EEPROM interface data out status		RO
74H	1	EDI	Direct program EEPROM interface data in status		RW
74H	2	ECK	Direct program EEPROM interface clock status		RW
74H	3	ECS	Direct program EEPROM interface chip select status		RW
74H	4	DPM	Direct program EEPROM mode		RW
74H	5	AUTOLD	Dynamic reload EEPROM content, the Ethernet ID will be updated.		RW
74H	6	EMBP	EEPROM embedded program enable, reset while programming complete		RW
74H	7	EEPR	EEPROM programmed status, 73H indicate programmed.		RO
75H	0-7	TEST	TEST mode register		RW
76H	0-7	DEGUG0	Debug mode 0		RW
77H	0-7	DEGUG1	Debug mode 1		RW

4-2-8. VT6102 internal register description (78-7BH)

OFFSET	Bit	Symbol	Description	Default	ACC
CFG_A					
78H	0-5	RESV	Reserved		RW
78H	6	MIIOPT	If MIIOPT=0,without extension clock. If MIIOPT=1, with extension clock.		RW
78H	7	EELOAD	Enable EEPROM embedded and direct programming , always 0 after power on and loading.		RW
CFG_B					
79H	0	LATMEN	Latency timer If LATMEN=0, Latency timer disable. If LATMEN=1, Latency timer enable		RW
79H	1	MWAIT	Master write insert one wait state 2-2-2-2		RW
79H	2	MRWAIT	Master read insert one wait state 2-2-2-2		RW
79H	3	RXARBIT	**Arbitration priority select.** The receive FIFO DMA will be interleave to transmitting FIFO DMA after 32 DWORD transaction		RW
79H	4	TXARBIT	The transmitting FIFO DMA will be interleave to Receiving FIFO DMA after 32 DWORD transaction		RW
79H	5	MRLDIS	**Memory read line support** If MRDLDIS=0, memory read line support If MRDLDIS=1, disable memory read line support		RW
79H	6	PERRDIS	Disable data parity generation and checking		RW
79H	7	QPKTDIS	Disable transmit frame queuing.		RW
CFG_C					
7AH	0	BPS0	**BOOTROM size select** 000----------no BOOTROM 001---------- 8K size 010----------16K size 011----------32K size 1xx----------64K size	000b	RW
7AH	1	BPS1			
7AH	2	BPS2			
7AH	3	BTSEL	BOOTROM timing select		RW
7AH	4	RESV	Reserved		RW
7AH	5	DLYEN	Turn on delay transaction while memory read bootrom.		RW
7AH	6	BROPT	Tie the unused bootrom address MA to high		RW
7AH	7	MED3	Medium select control		RW
CFG_D					
7BH	0	BAKOPT	Backoff algorithm optional If BAKOPT=0,disable Backoff algorithm optional If BAKOPT=1,enable Backoff algorithm optional	0	RW
7BH	1	MBA	Capture effect solution selection -1 for AMD solution	0	RW
7BH	2	CAP	Capture effect solution select-2 for DEC solution	0	RW
7BH	3	CRADOM	Backoff algorithm random.	0	RW
7BH	4	PMCDIG	PMCC(0x82) setting test mode, while PMCCDIG=1 can be read/write.	0	RW
7BH	5	MRLEN	**PCI memory read line capable.** If MRLEN=0, no capable. If MRLEN=1, capable.	0	RW
7BH	6	DIAG	Diagnostic mode If DIAG=0, disable. If DIAG=1, enable .	0	RW
7BH	7	MMIOEN	Memory mapped IO access enable.	0	RW

4-2-9. VT6102 internal register description (80-8BH)

OFFSET	Bit	Symbol	Description	Default	ACC
MISC.CR					

80H	0	Tm0EN	Enable software timer 0 to count		RW
80H	1	Tm0Susp	Tm0susp will be set 1, when SoftTimer0 time out When SW clear Tm0susp to 0, SoftTimer0 will continue to Count.		RW
80H	2	HDXFEN	Half-duplex flow control enable		RW
80H	3	FDXRFEN	Full-duplex flow control RX enable		RW
80H	4-7	RESV	Reserved		RW
81H	0	Tm1EN	Enable software timer 1 to count		RW
81H	1-4	RESV	Reserved		RW
81H	5	VAXJMP	There is a AUX power outside, for software reference		RW
81H	6	FORSRST	Force software reset		RW
81H	7	RESV	Reserved		RW
STICKHW					
83H	0	DS0	Sticky DS0_shadow,suspend well DS write port		RW
83H	1	DS1	Sticky DS1_shadow, R/W by software		RW
83H	2	WOLEN	Legacy WOL enable		RW
83H	3	WOLSR	Legacy WOL status		RW
83H	4-6	RESV	Reserved		RW
83H	7	LGWOL	Legacy WOL enable ,status for software reference from jumper strapping MD5.		RW
MISR					
84H	0	TM0INT	Software timer o interrupt		RW
84H	1	TM1INT	Software timer 1 interrupt		RW
84H	2	RESEV	Reserved		RW
84H	3	TDWBR	TD WB queue race, will cause when TX shut down.		RW
84H	4	SSRCI	Suspend well MII polling status change interrupt.		RW
84H	5	UDPIS	User defined, host driven interrupt		RW
84H	6	UDPI	User defined, host driven interrupt		RW
84H	7	PWEI	Power event report in test mode		RW
85H	0-7	RESV	Reserved		RW
MIMR					
86H	0	TM0IM	Software timer o interrupt mask		RW
86H	1	TM1IM	Software timer 1 interrupt mask		RW
86H	2	RSEV	Reserved		RW
86H	3	TDWBIM	TD WB queue race, will cause when TX shut down mask		RW
86H	4	SSRCIM	Suspend well MII polling status change interrupt, by diagnosis use mask		RW
86H	5	0	User defined, host driven interrupt mask		RW
86H	6	UDPIM	User defined, host driven interrupt mask		RW
86H	7	PWEIM	Power event report in test mode mask		RW
87H	0-7	RESV	Reserved		RW
88-8BH	0-31	RESV	Reserved		RW

4-2-10. VT6102 internal register description (8C-A7H)

OFFSET	Bit	Symbol	Description	Default	ACC
BPMA[15:0]					
8C-8DH	0-15	BPMA	Flash address port [15:0]		RW
8EH	0-7	RESV	Reserved		RW
8FH	0-7	BPMD	Flash write data output port		RW
BPCMD					
90H	0	EBPRD	BOOTROM embedded read command		RW
90H	1	EBPWR	BOOTROM embedded write command		RW
90H	2-6	RESV	Reserved		RW
91H	0-7	BPIN	Flash write data output port		RW
92H	0-7	RESV	Reserved		RW
93H	0-7	CHKSUM	EE_CHKSUM		RW
94-95H	0-15	Suspend MII_AD	MII address at suspend well		RW
96H	0-7	SU_PHYID	PHY address at suspend well		RW
97H	RESV	0-7	Reserved		RW
98-99H	0-15		Pause timer		RW
9A-9BH	0-15		PauseSR		RW
9C-9DH	0-15		Soft timer_0 period		RW
9E-9FH	0-15		Soft timer_1 period		RW
WOLCR.SET / WOLCR.CLR					
A0/A4H	0-3	PTNMH	PTNMH[3:0] enable pattern match filtering		RW
A0/A4H	4	UNICAST	Enable UNICAST filter.		RW
A0/A4H	5	MAGICEN	Enable Magic packet filter.		RW
A0/A4H	6	LinkON	Enable link on detected .		RW
A0/A4H	7	LinkOFF	Enable link off detected.		RW
PWCFG.SET /PWCFG.CLR					
A1/A5H	0	WOLEN	Legacy WOL_EN shadow		RW
A1/A5H	1	WOLSR	Legacy WOL_SR shadow		RW
A1/A5H	2-3	RESV	Reserved		RW
A1/A5H	4	LEGCY WOL	Enable legacy wake on lan		RW
A1/A5H	5	WOLTYPE	Drive WOL output by pulse(1) or button (0)		RW
A1/A5H	6	RESV	Reserved		RW
A1/A5H	7	SMIITIME	Internal MII interface timing		RW
TESTREG.SET / TESTREG.CLR					
A2/A6H	0	SNORM	All power state capable while PHYTEST=0		RW
A2/A6H	1-7	RESV	Reserved		RW
WOLCG.SET / WOLCG.CLR					
A3/A7H	0-1	RESV	Reserved		RW
A3/A7H	2	SMIIOPT	MIIOPT to extend clock in suspend well		RW
A3/A7H	3	SMIIACC	MDC acceleration		RW
A3/A7H	4	SAB	Accept broadcast in suspend well		RW
A3/A7H	5	SAM	Accept multicast in suspend well		RW
A3/A7H	6	SFDX	Full duplex in suspend well		RW
A3/A7H	7	PMEOVR	For legacy use, force PMEEN always over PME_EN		RW

4-2-11. VT6102 internal register description (B0-FFH)

OFFSET	Bit	Symbol	Description	Default	ACC
PATTERN CRC0-CRC3					
B0-B3H	0-31	CRC0	PATTERN CRC0		RW
B4-B7H	0-31	CRC1	PATTERN CRC1		RW
B8-BBH	0-31	CRC2	PATTERN CRC2		RW
BC-BFH	0-31	CRC3	PATTERN CRC3		RW
BYTEMSK 0-3					
C0-CFH	0-127	Bytemsk	BYTEMSK 0		RW
D0-DFH	0-127	Bytemsk	BYTEMSK 1		RW
E0-EFH	0-127	Bytemsk	BYTEMSK 2		RW
F0-FFH	0-127	Bytemsk	BYTEMSK 3		RW

5. ELECTRICAL SPECIFICATION

5-1. ABSOULTE MAXIMUN RATING

Parameter	Min	Max	Unit
Supply Voltage	3.0	3.6	Volts
Input Voltage	-0.5	Vcc+0.5	Volts
Output Voltage	-0.5	Vcc+0.5	Volts
Storage Temperature	-65	150	¢ J
Ambient Temperature	0	70	¢ J
ESD Rating	-	2500	Volts

Note: Stress above the conditions listed may cause permanent damage to the device Functional operation of this device should be restricted to the conditions described Under operating conditions.

5-2. DC SPECIFICATIONS

TA-0-70¢ ,JVcc =3.3V

Symbol	Parameter	Min	Max	Unit	Condition
ICC	Supply Current – Average Active	-	100	mA	X1=25Mhz, VIN switching
ICCIDLE	Supply Current – Average Idle	-	80	mA	X1=25Mhz, VIN=Vcc or GND
ICCLP	Supply Current – Low Power Mode	-	35	mA	X1 undriven, VIN=Vcc or Undriven
VIL	Input Low Voltage	-0.5	0.8	V	
VIH	Input High Voltage	2.0	Vcc+.05	V	
IIL	Input Leakage Current	-1.0	+1.0	uA	GND<VIN<Vcc
VOL	Output Low Voltage – High Drive Outputs	-	0.5	V	IOL= 20uA
VOH	Output High Voltage – High Drive Outputs	2.4	-	V	IOH= -20uA
VOLM	Output Low Voltage – MOS Outputs	-	0.1	V	IOL= 20uA
VOHM	Output High Voltage – MOS Outputs	-	Vcc-0.1	V	IOH= -20uA
VOL	Output Low Voltage – O.C. Output	-	0.5	V	IOL= 24uA
IOZ	Tristate Leakage Current	-10	+10	uA	GND<VOUT<Vcc

Note: These parameters are not guaranteed by production testing, All electrical specification are based on IEEE 802.3 requirements and internal design considerations.

6. TIMING SPECIFICATION

6-1. PCI BUS MASTER

1.All of the timing are captured from verilog simulation with three cases : Best/Normal/Worst
2.PCICLK = 33MHz

6-1-1. Get TX descriptor

Symbol	Parameter	Width (ns)	Note
tfval	PCICLK rising edge to FRAME# Valid Delay	(7.2, 10.6, 18.7)	
tadval	PCICLK rising edge to AD[31:0] Valid Delay	min:(7.7, 11.1, 20.0), max:(8.6, 12.7, 22.3)	
tcbeval	PCICLK rising edge to CBE[3:0] Valid Delay	(4.7, 7.0, 12.2)	
tirval	PCICLK rising edge to IRDY# Valid Delay	(4.7, 7.0, 12.2)	
tfhold	FRAME# hold time	(6.9, 10.2, 18.0)	2.
tirhold	IRDY# hold time	(3.2, 4.8, 8.4)	3.

Note :
1.(xxx, xxx, xxx) : (best, normal, worst)
2.FRAME# hold time for frame#=0 to frame#1
3.IRDY# hold time for frame#=0 to frame#1

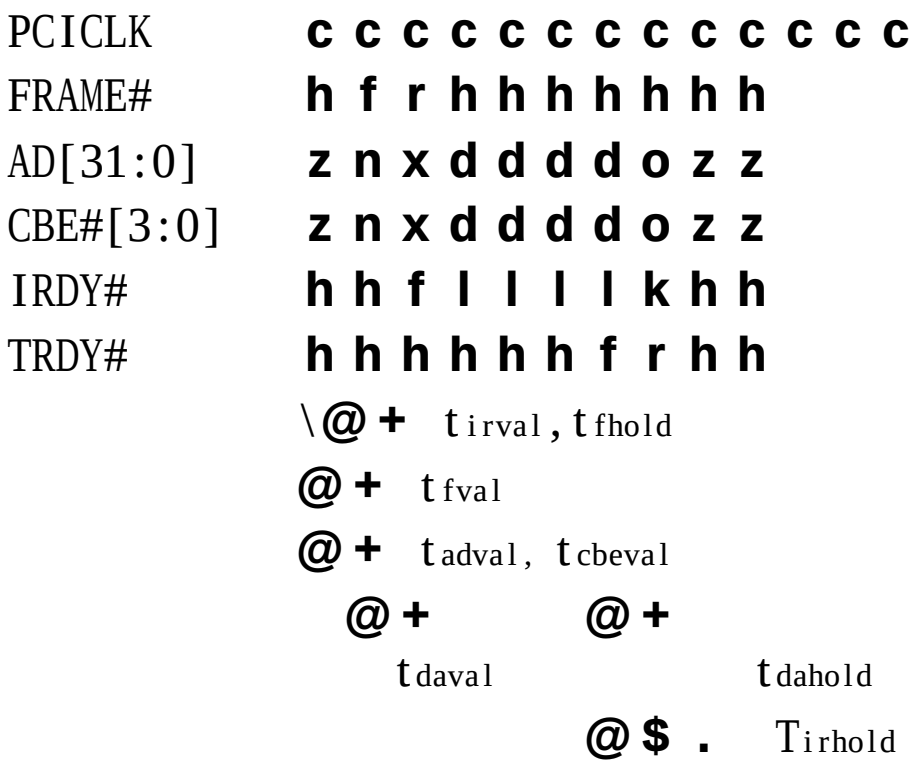
6-1-2. Get RX descriptor

Symbol	Parameter	Width (ns)	Note
tfval	PCICLK rising edge to FRAME# Valid Delay	(7.2, 10.6, 18.7)	
tadval	PCICLK rising edge to AD[31:0] Valid Delay	min:(7.7, 11.1, 20.0), max:(8.6, 12.7, 22.3)	
tcbeval	PCICLK rising edge to CBE[3:0] Valid Delay	(4.7, 7.0, 12.2)	
tirval	PCICLK rising edge to IRDY# Valid Delay	(4.7, 7.0, 12.2)	
tfhold	FRAME# hold time	(7.0, 10.3, 18.2)	2.
tirhold	IRDY# hold time	(3.2, 4.8, 8.4)	3.

Note :

1.(xxx, xxx, xxx) : (best, normal, worst)
2.FRAME# hold time for frame#=0 to frame#1
3.IRDY# hold time for frame#=0 to frame#1

6-1-3. Write back status to descriptor

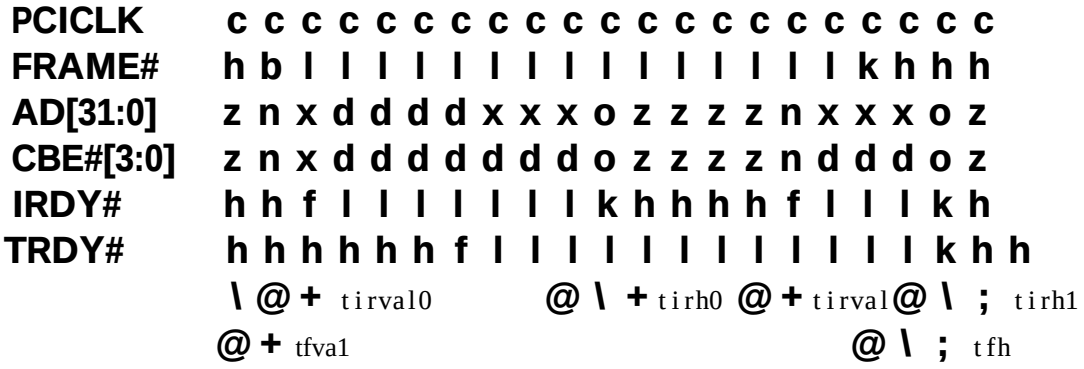


Symbol	Parameter	Width (ns)	Note
tfval	PCICLK rising edge to FRAME# Valid Delay	(7.2, 10.6, 18.7)	
tadval	PCICLK rising edge to AD[31:0] Valid Delay	(7.7, 11.4, 20.0)	
tcbeval	PCICLK rising edge to CBE[3:0] Valid Delay	(4.7, 7.0, 12.2)	
tirval	PCICLK rising edge to IRDY# Valid Delay	(4.7, 7.0, 12.3)	
tfhold	FRAME# hold time	(5.7, 8.4, 14.8)	
tdaval	PCICLK rising edge to AD[31:0](data) Valid Delay	(7.2, 10.6, 18.7)	
tfhold	FRAME# hold time	(5.7, 8.4, 14.8)	
tdahold	AD[31:0] hold time	(5.2, 7.6, 13.4)	
tirhold	IRDY# hold time	(3.2, 4.8, 8.4)	

Note :

1.(xxx, xxx, xxx) : (best, normal, worst)

6-1-4. Read data into FIFO

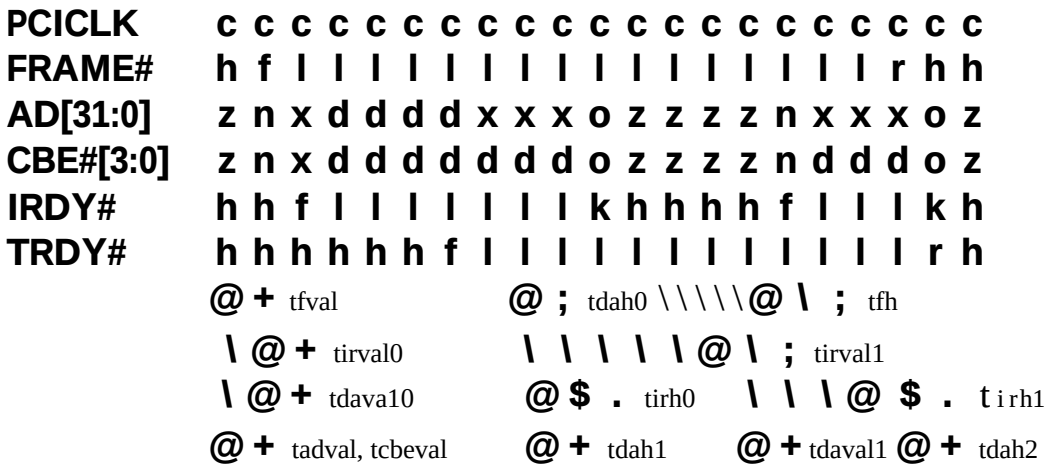


Symbol	Parameter	Width (ns)	Note
tfval	PCICLK rising edge to FRAME# Valid Delay	(7.2, 10.6, 18.7)	
tfh	FRAME# hold time	(6.9, 10.2, 17.9)	
tirval0	PCICLK rising edge to IRDY# Valid Delay	(4.7, 7.0, 12.3)	
tirval1	PCICLK rising edge to IRDY# Valid Delay	(4.8, 7.0,12.4)	
tirh0	IRDY# hold time	(3.5, 5.1, 8.9)	
tirh1	IRDY# hold time	(3.2, 4.8, 8.4)	
tadval	PCICLK rising edge to AD[31:0] Valid Delay	min(7.7, 11.4, 20.0), max(9.5, 13.9, 24.5)	
tcbeval	PCICLK rising edge to CBE[3:0] Valid Delay	(4.7, 7.0, 12.3)	

Note :

1.(xxx, xxx, xxx) : (best, normal, worst)

6-1-5. Write data from FIFO



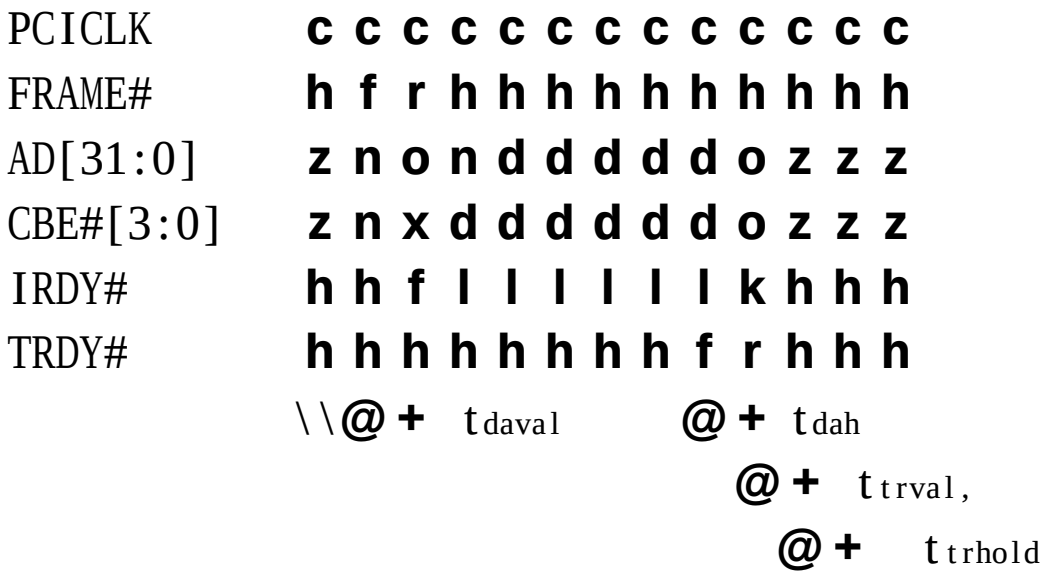
Symbol	Parameter	Width (ns)	Note
tfval	PCICLK rising edge to FRAME# Valid Delay	(7.2, 10.6, 18.7)	
tfh	FRAME# hold time	Min.(6.8, 9.9, 17.5) Max(7.6, 11.2, 19.7)	
tirval0	PCICLK rising edge to IRDY# Valid Delay	(4.7, 7.0, 12.3)	
tirval1	PCICLK rising edge to IRDY# Valid Delay	(5.3, 7.9, 13.8)	
tadval	PCICLK rising edge to AD[31:0] Valid Delay	Min(7.7, 11.4, 20.0) Max(9.5, 13.9, 24.5)	
tcbeval	PCICLK rising edge to CBE[3:0] Valid Delay	(4.7, 7.0, 12.2)	
tirh0	IRDY# hold time	(4.0, 5.8, 10.3)	
tirh1	IRDY# hold time	(3.2, 4.8, 8.4)	
tdaval0	PCICLK rising edge to data Valid Delay	Min(4.9, 7.2, 10.7) Max(7.2, 10.6, 18.6)	
tdaval1	PCICLK rising edge to data Valid Delay	Min.(5.1, 7.6, 13.3) Max(7.7, 11.1, 19.5)	
tdah0	Data hold time	Min.(4.3, 6.4, 11.2) Max.(7.4, 10.9, 19.2)	
tdah1	Data hold time	Min.(4.3, 6.4, 11.2) Max.(5.1, 7.6, 11.5)	
tdah2	Data hold time	Min.(4.3, 6.5, 11.5) Max.(5.2, 7.9, 13.4)	

Note :

1.(xxx, xxx, xxx) : (best, normal, worst)

6-2. PCI BUS SLAVE

6-2-1. IO read/write

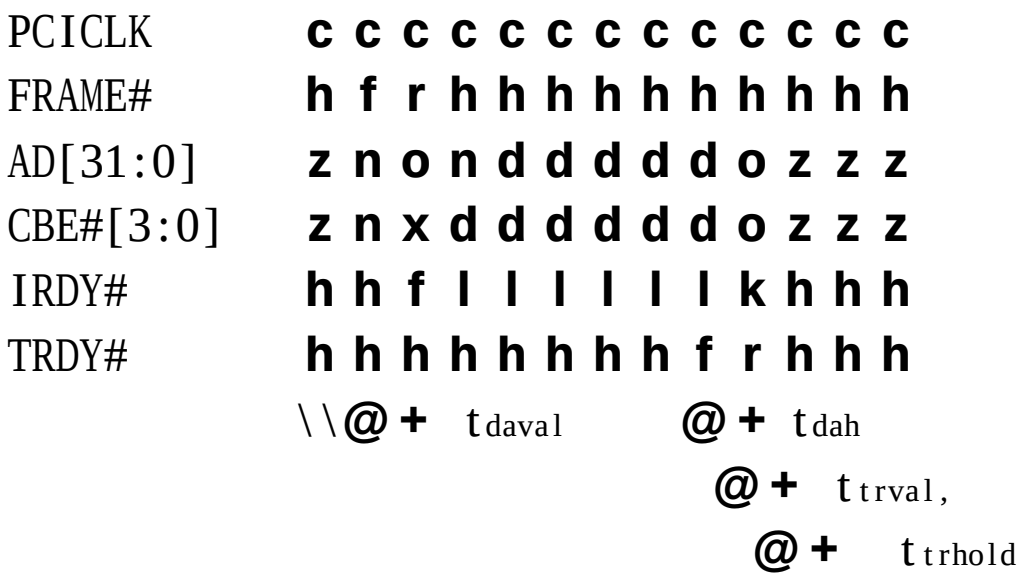


Symbol	Parameter	Width (ns)	Note
tdaval	PCICLK rising edge to DATA Valid Delay	Max.(8.2, 12.1, 21.3) Min(5.8, 8.5, 15.0)	2
tdah	DATA hold time	Max(8.4, 12.1, 21.9) Min(5.8, 8.5, 15.0)	2
ttrval	PCICLK rising edge to TRDY# Valid Delay	(4.6, 6.7, 11.8)	
ttrh	TRDY# hold time	(3.1, 4.6, 8.2)	

Note :

1.(xxx, xxx, xxx) : (best, normal, worst)
2. IO read only

6-2-2. Cfg read/write



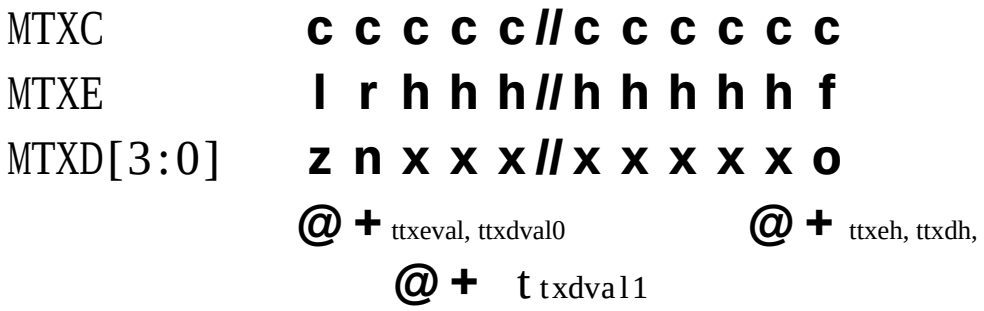
Symbol	Parameter	Width (ns)	Note
tdaval	PCICLK rising edge to DATA Valid Delay	(8.2, 12.1, 21.3)	2
tdah	DATA hold time	(5.8, 8.5, 15.0)	2
ttrval	PCICLK rising edge to TRDY# Valid Delay	(4.6, 6.7, 11.8)	
ttrh	TRDY# hold time	(3.1, 4.6, 8.2)	

Note :

1.(xxx, xxx, xxx) : (best, normal, worst)
2.Cfg read only

6-3. MII

6-3-1. MII TX



Symbol	Parameter	Width (ns)	Note
ttxeval	PCICLK rising edge to TXE Valid Delay	(3.7, 5.4, 9.5)	
ttxdval0	PCICLK rising edge to TXD Valid Delay	(3.6, 5.3, 9.3)	
ttxdval1	PCICLK rising edge to TXD Valid Delay	Min.(3.5, 5.1, 8.9) Max.(5.8, 8.6, 15.1)	
ttxeh	TXE hold time	(5.9, 8.7, 15.3)	
ttxdh	TXD hold time	(5.7, 8.4, 14.7)	

Note :

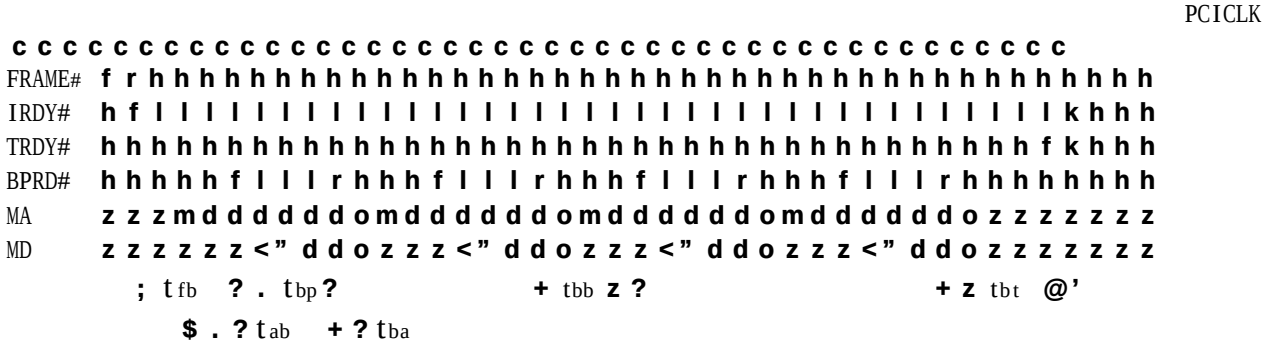
1.(xxx, xxx, xxx) : (best, normal, worst)

6-3-2. MII MDIO

All of MDIO signals transition occure in negative egde of MDC.

6-4. BOOTROM

6-4-1. One Dword bootrom access timing (with delay transaction)

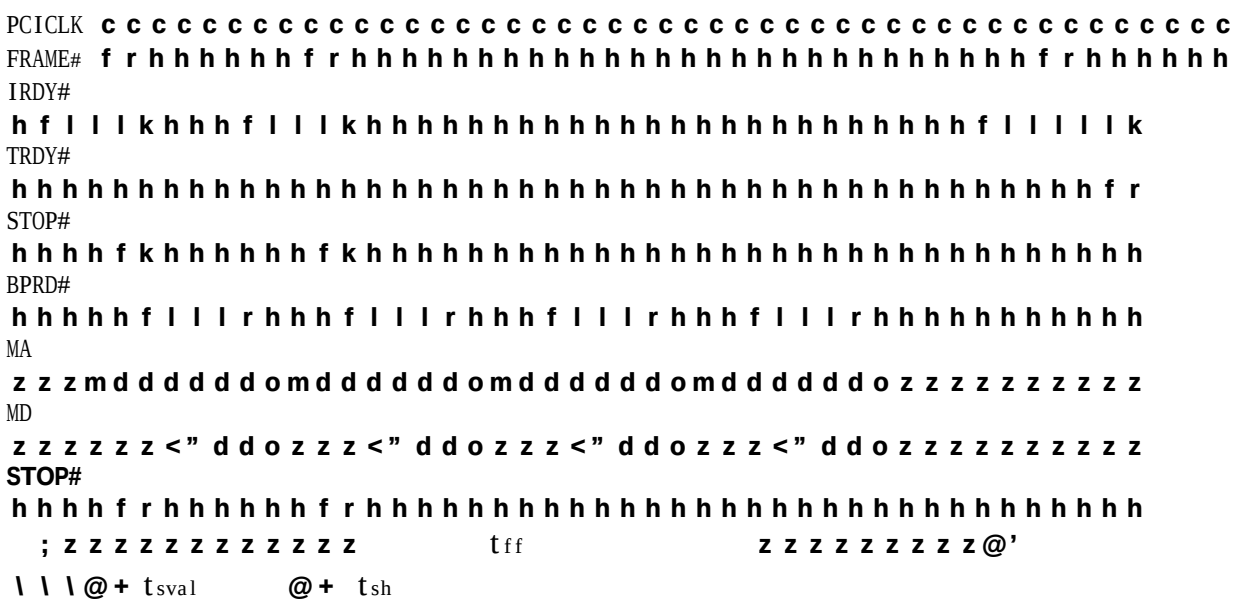


Symbol	Parameter	max (ns)	min (ns)	Note
tfb	The PCLK rising edge which latches FRAME# to BPRD# is asserted		(485, 487, 492)	2
tab	MA ready to BPRD# asserted		(29.5, 29.4, 28.9)	
tbp	BPRD# is asserted	(509, 508, 508) (DTSEL=1)	(299,298,298) (DTSEL=0)	3,
tba	BPRD# deasserted to MA deasserted		(29.7, 29.5, 29.2)	
tbb	BPRD# is deasserted between two one byte bootrom cycle		(510, 511, 512)	
tbt	BPRD# is deasserted to the PCLK rising edge which latches TRDY#		(145, 143, 139)	

Note :

1.Delay transaction control bit : PCI cfg/7ah/bit5
2.(xxx, xxx, xxx) : (best, normal, worst)
3.DTSEL : PCI cfg/7ah/bit4

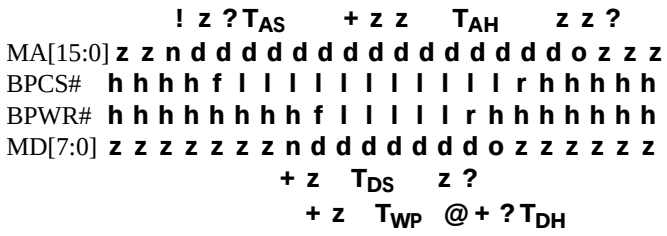
6-4-2. One Dword bootrom access timing (without delay transaction)



Symbol	Parameter	(ns)	Note
tff	The initial FRAME# to the second valid FRAME#	min (3300, 3300, 3300)	
tsval	PCICLK rising edge to STOP# Valid Delay	(5.4, 8.0, 14.1)	
tsh	STOP# hold time	(3.8, 5.6, 9.8)	

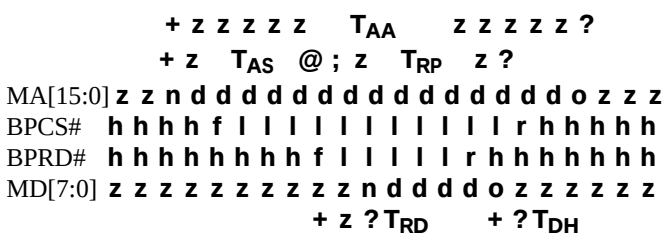
6-4-3. Embedded Flash Cycle Timing

A. Flash Write Timing, WE# controlled only:



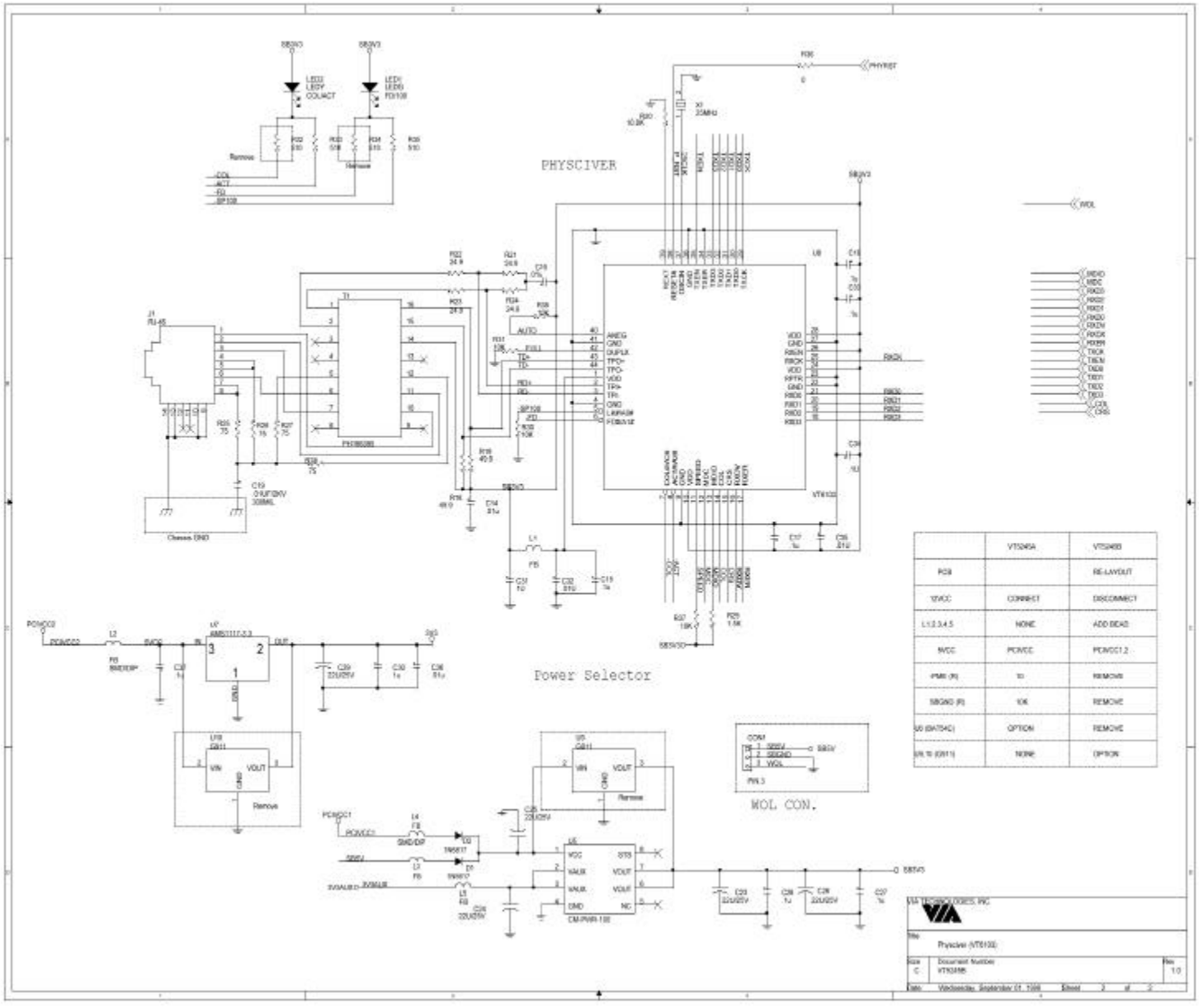
Symbol	Parameter	Timing	Unit
T_{AS}	Address Setup Time	116	ns
T_{AH}	Address Hold Time	423	ns
T_{WP}	BPWR# Pulse Width	270	ns
T_{DS}	Data Setup Time	298	ns
T_{DH}	Data Hold Time	61	ns

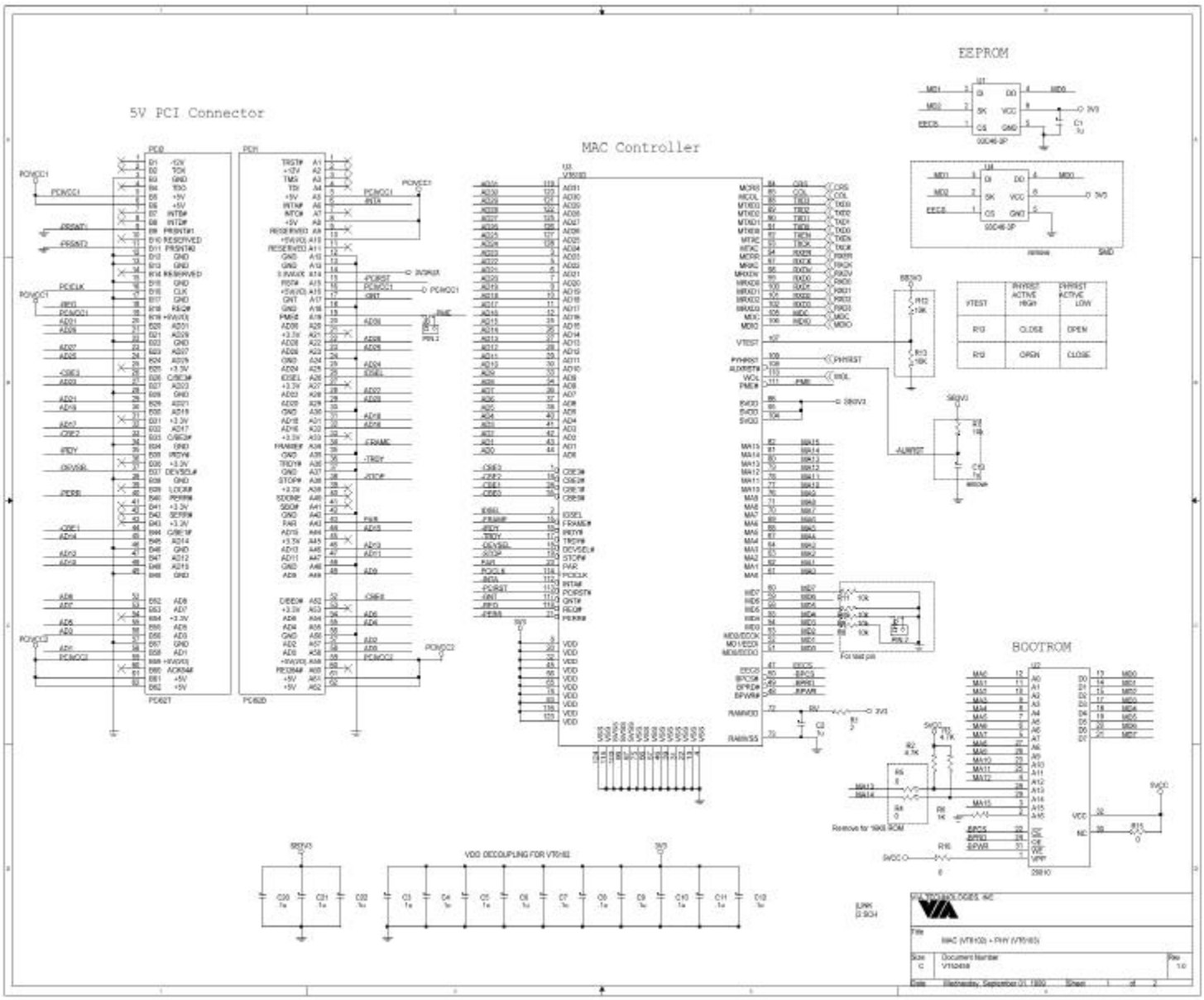
B. Flash Read Timing:



Symbol	Parameter	Timing	Unit
T_{AS}	Address Setup Time	85	ns
T_{AA}	Address Cycle Time	508	ns
T_{RP}	BPRD# Pulse Width	330	ns
T_{RD}	Read Access Time	230(max)	ns
T_{DH}	Data Hold Time	0 (max)	ns

7. APPLICATION SCHEMATIC




EEPROM
5V PCI Connector
MAC Controller
BOOTROM
VDD DECOUPLING FOR VT6102

8. Package Mechanical Specifications